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Development of Large-Area Monolithically Integrated Silicon-Film Photovoltaic Modules

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1. Introduction

The objective of this program is to develop Silicon-Film Product III into a low cost, stable device for large scale terrestrial power applications. The Product III structure is a thin (<100μm) polycrystalline silicon layer on a non-conductive supporting ceramic substrate (see Figure 1). The presence of the substrate allows cells to be isolated and interconnected monolithically in various series/parallel configurations. The long term goal for the product is efficiencies over 18% on areas greater than 1200 cm^2. The high efficiency is made possible due to the benefits of utilizing polycrystalline thin silicon incorporated into a light trapping structure with a passivated back surface. Short term goals are focused on the development of large area ceramics, a monolithic interconnection process, and fabricating 100 cm^2 solar cells.

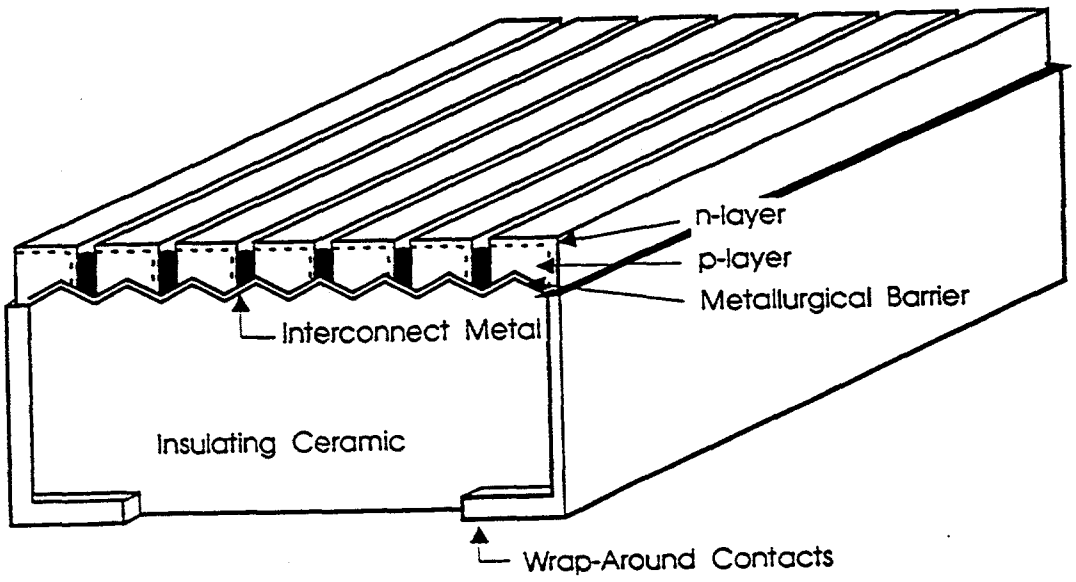


Figure 1. Silicon-Film Product III showing series interconnected silicon devices on an insulating substrate.

1.1 Background

The Silicon-Film process development, guided by device modeling will achieve a high performance solar cell structure based on imperfect materials. The specific technical approach involves the deposition of thin silicon layers on a rigid ceramic substrate. The commercial feasibility of this approach has been demonstrated by the achievement of a 100 cm^2, 10.9% commercial-size solar cell [1]. The potential of this approach is further established by the achievement of a 1.0 cm^2, 15.7% Si-Film solar cell [2].

The development of the Silicon-Film process has generated a family of three products. They are pictured in **Figure 2.** Product I, presently in production, utilizes a 100 μm thick active layer of silicon on a low cost supporting substrate. There is no metallurgical barrier layer between the active layer and the substrate. Light trapping features are limited.

Light trapping is incorporated into the Product II design shown in **Figure 2.** Product II is enhanced from Product I by: (1) the presence of an optically reflecting metallurgical barrier layer, (2) surface texture designed for light trapping, and (3) by the reduction in thickness of the active silicon layer (30 μm).

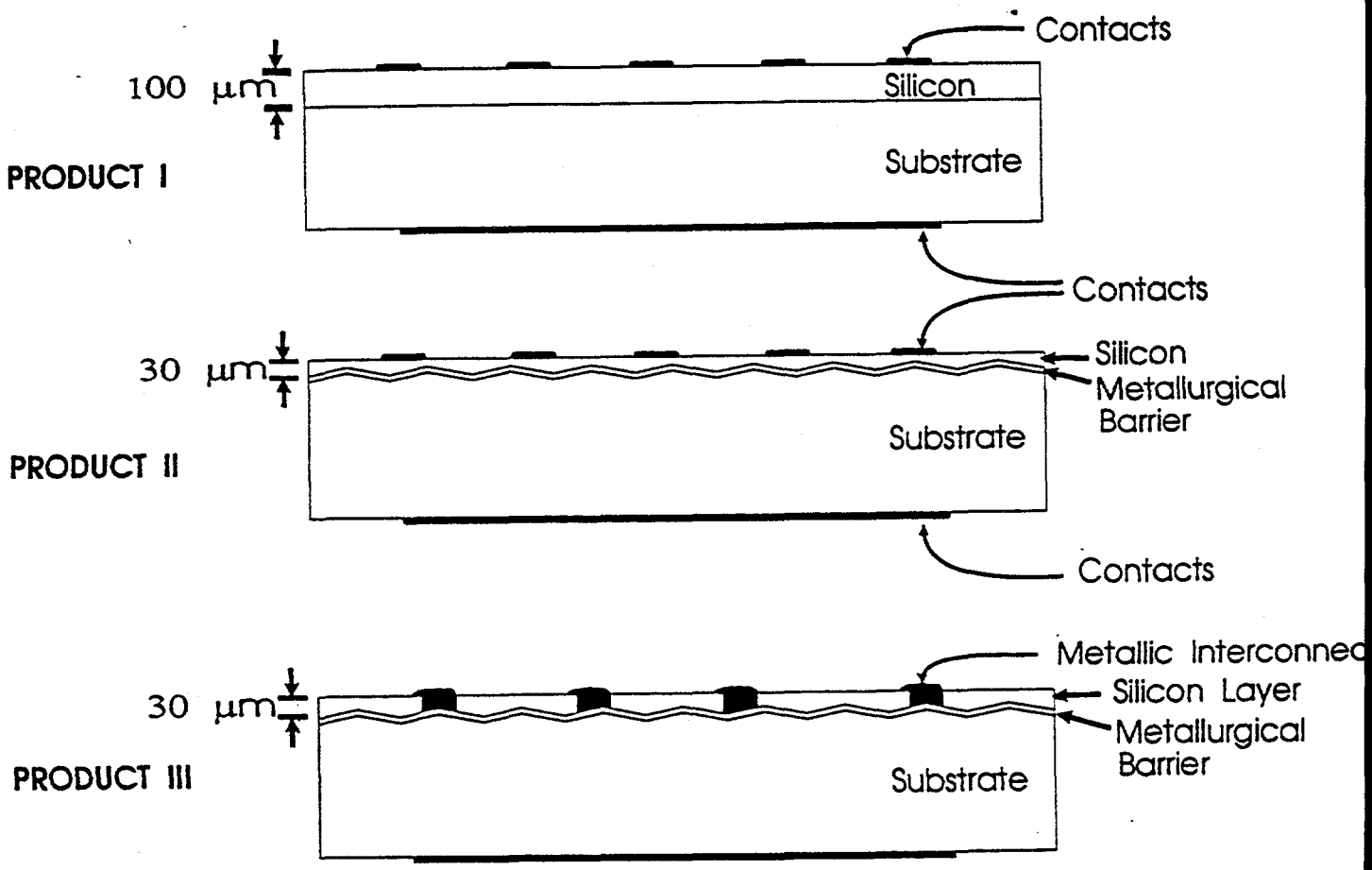


Figure 2. The Silicon Film product families.

Product III utilizes the Silicon-Film process developed for Product II, therefore enjoying the performance and cost benefits of the thin silicon light trapping design. The active silicon layer is configured into a monolithically interconnected, high-voltage structure on an insulating ceramic. The effort described here is involved with only the development of the Product III device.

1.2 Device Modeling

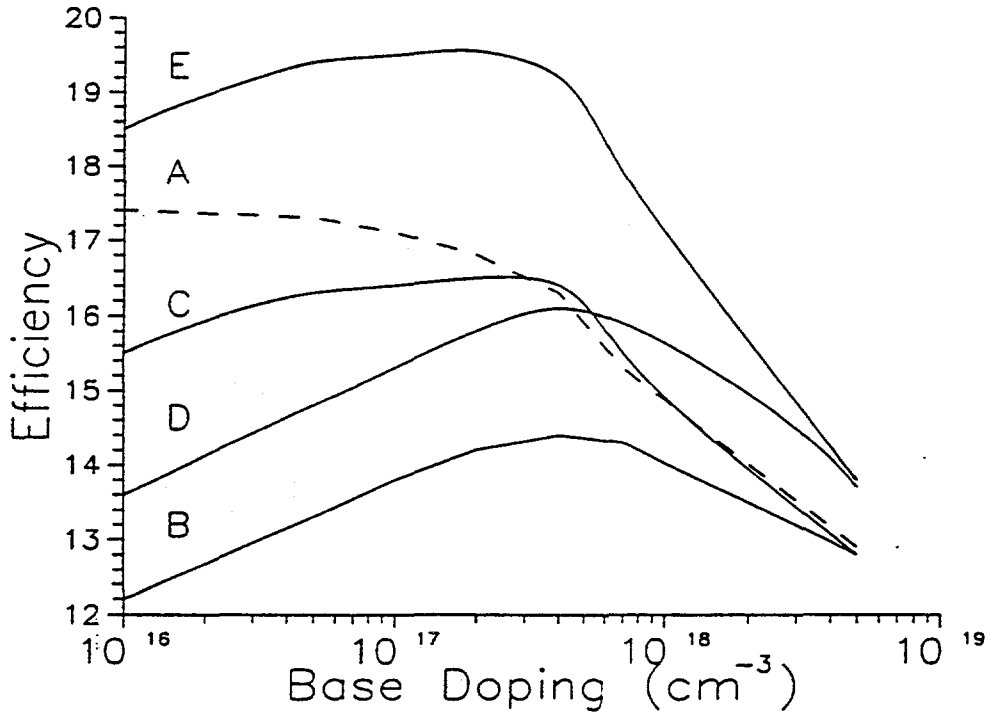
The Silicon-Film design achieves high performance through the utilization of a thin silicon layer. Optimally designed thin crystalline solar cells (<50 μm thick) have performance advantages over conventional thick devices. The enhancement in performance requires device designs to incorporate back surface passivation and light-trapping. The effects of light trapping and back surface passivation on overall device energy conversion efficiency are shown in **Figure 3**. This modeling method highlights the limited dependence of the performance of Silicon-Film devices on silicon quality and minority carrier diffusion length. **Figure 3** shows that the efficiency of a 35 μm thick device with both light trapping and back surface passivation is superior to that of a conventional device at all doping levels of interest. Peak efficiencies for the thin device are predicted for doping levels in the range of $2x10^{17}$ cm^{-3} to $5x10^{17}$ cm^{-3}. These doping levels correspond to diffusion lengths in the range of 40 μm to 80 μm. The efficiencies of the thin devices are predicted to decrease as base doping is decreased. This is a result of decreasing V_{oc} that occurs at lower doping levels. The same effect occurs in the conventional device, however current increases offset the lower V_{oc} values, and efficiency remains constant.

The limited dependence on diffusion length allows the thin device to use higher base doping levels and therefore achieve high V_{oc}. This option is not available to thick conventional devices as long diffusion lengths are required to collect minority carriers generated deep in the base layer. The long diffusion length requirement in conventional devices allows high efficiency to be obtained only with high quality, relatively expensive single crystal silicon wafers.

Device Modeling

Model Parameters

		S_{BACK}	Optical Path Length
A -	400μm Thick Conventional Device	10^6 cm/s	Z = 1
B -	35μm Thick Conventional Device	10^6 cm/s	Z = 1
C -	35μm Thick Device with Back Surface Passivation	10^3 cm/s	Z = 1
D -	35μm Thick Device with Light-Trapping	10^6 cm/s	Z = 20
E -	35μm Thick Device with Light-Trapping and Back Surface Passivation	10^3 cm/s	Z = 20



Effects of light-trapping and back surface passivation on the efficiency (AM1.5G) of thin (35μm) and thick (400μm) silicon devices.

Figure 3. Predicted conversion efficiency (AM1.5G) as a function of base doping. Diffusion lengths are adjusted to be consistent with doping levels.

1.3 Device Design

The thin (<50 μm) active silicon layers used in the Silicon-Film products are ideally suited to the task of monolithic integration. The major elements of the Product III structure (as pictured in **Figures 1 and 4**) have already been developed for Products I and II. These elements are the ceramic, the barrier layer, the thin silicon layer, and textured surfaces for light trapping. This will allow the Product III effort to focus on the differences a monolithic interconnection scheme will make during device fabrication. The elements of the proposed Product III device that require development work are reviewed in section **2.1 - Scope of Research Effort**.

The Product III module, submodule, and cell interconnection are shown in **Figure 4**. The use of monolithic interconnection provides the following advantages:

1. All cell interconnections are done as part of the submodule fabrication process.

2. High module voltages can be obtained.

3. The efficiency and stability of crystalline silicon can be obtained in large area, low cost, monolithically integrated submodules.

4. All submodule interconnections can be made on the back of the ceramic substrates.

5. The substrates can be made large enough to span the width of the module (as shown in **Figure 4**).

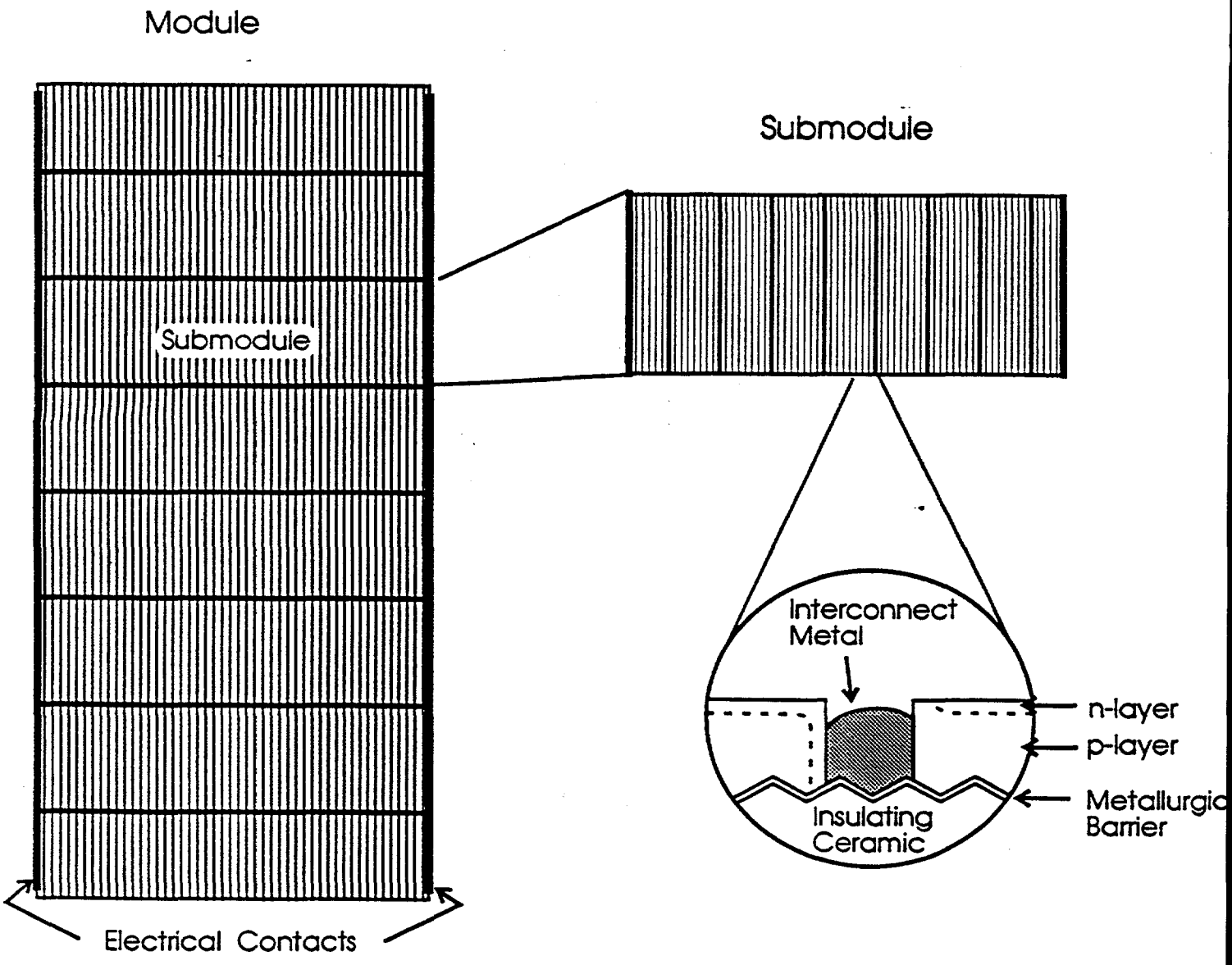


Figure 4. Product III module, submodule, and cell interconnection.

2.0 Objectives

The objective of the proposed work is to develop Si-Film Product III into a low cost, stable, device for large scale terrestrial power applications. The long term goal for the product is efficiencies over 18% on areas greater than 1200 cm^2. Cell interconnections will be made monolithically on ceramic substrates. A significant enhancement to efficiency will come from device designs that involve no grid obscuration.

The proposed work can be separated into 7 areas. These individual areas and near term objectives are discussed below.

2.1 Large Area Ceramic Development

Ceramic substrates have been developed for the present Product II effort. They have been developed, and are fabricated, in-house at AstroPower. The present fabrication sequence involves formulating the ceramic composition, tape casting into substrates (10 cm X 50 cm X 0.05 cm), sizing to 100 cm^2, and high temperature sintering. The ceramic presently being used in the Product II effort has been formulated from readily available, low cost materials.

Through the development of this ceramic at AstroPower, significant expertise has been developed. This expertise has led to the ability to control ceramic properties such as; thickness uniformity, thermal properties, electrical conductivity, and surface texture. The resistivity of the ceramic is presently designed to be 0.5 to 2.0 Ω-cm to provide electrical back contact on the Product II structure. Conductivity requirements for the Product III structure are different. Ceramic development work has lead to substrates with electrically insulating properties.

Other development work has included increasing the final ceramic size from 100 cm^2 to 500 cm^2. The increases in size will require upgrades to the processes and equipment used for ceramic fabrication. Research and development of localized areas of conduction will also be undertaken. Localized conduction will lead to wrap-around back contacts (making an all back contact device for ease of interconnection).

2.2 Metallurgical Barrier Materials and Deposition

A metallurgical barrier (MB) is incorporated into the present Product II device. The barrier must play a number of critical roles in the physical and electrical nature of the device. Physically, the barrier must protect the active layer from impurities within the ceramic, and be reflective to long wavelength light trapped in the active layer. Electrically, the barrier must provide a low recombination back surface to the active layer, and allow for ohmic back contact (for the PII structure). The only barrier property that must be altered for the Product III structure is the electrical conduction properties. Initially the barrier-ceramic system will be made insulating (insulating barrier materials have been demonstrated). Conducting back planes (as discussed in Section 2.1D) will require further development of the barrier properties.

2.3 Light Trapping Enhancements

To increase absorption of long wavelength light in thin Si-Film active layers, light trapping will be used. Detailed analysis of light trapping structures has been undertaken. The general light trapping structures required for Product III will be similar

to those developed for Product II. Through the use of back surface texturing (either random or regular) and metallurgical barriers of carefully designed reflective properties, high levels of light trapping have been achieved. The level of light trapping can be quantified by Z, the optical path length of the light given as a multiple of the device thickness. Optical properties have been measured in the present PII structure to show a Z=9 has been achieved [3].

2.4 Back Surface Conduction

Contacting methods for the proposed Product III design have been developed. Present designs call for metal systems that interconnect silicon p-layers to neighboring n-layers. Development of the interconnection scheme is covered in Section 4, Device Processing Results. The cell size will be limited by resistive losses within the cell. Higher cell conduction in the n-layer can be achieved by the use of grids on the front surface. Increased p-layer conduction can be achieved by the use of a back plane conductor. The development of a back plane conductor will require altering the barrier system to allow for the addition of a conducting plane beneath each cell. Care must be taken in the interconnection scheme to eliminate the possibility of shunting. A generalized schematic of the back plane conductor is shown in **Figure 5.**

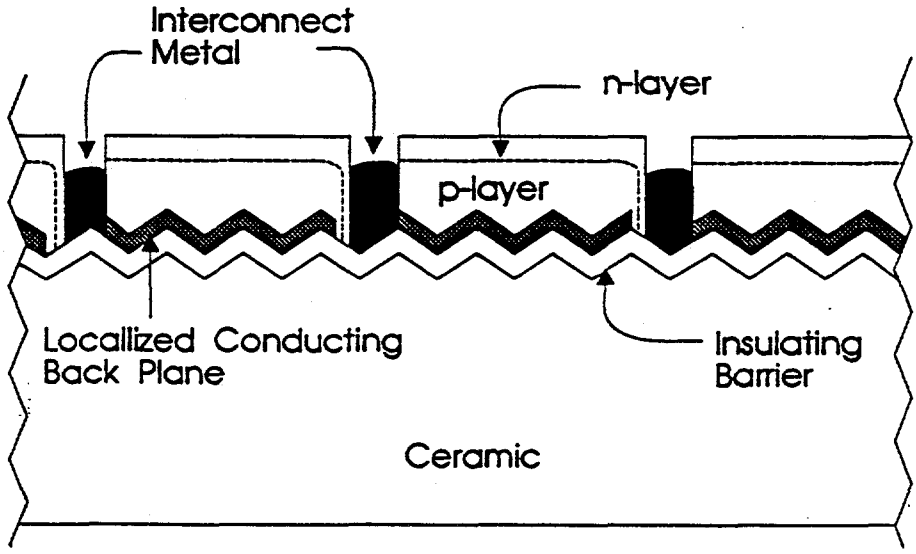


Figure 5. Cross section on a Product III device showing back plane conduction assisted by a back plane conductor.

2.5 Silicon Deposition

Silicon active layers are grown from a solution. The processes used for the present Product II program are directly applicable to the Product III device. The deposition systems have been scaled-up to account for increases in overall submodule size.

2.6 Monolithic Integration

The ability to interconnect cells into an integrated array will be developed. A key element in achieving such a structure is the ability to isolate areas of the submodule (i.e. Si-Film wafer) into cells. The fact that the active device is only 20 to 50 microns thick and is supported by an insulating barrier-ceramic substrate allows this to occur. A contacting scheme has been designed to retrieve the generated power in any I-V configuration required. All electrical contacts are applied on the top of the device. **Figure 1** shows one possible interconnection scheme. The process sequence to achieve such a configuration is reviewed in detail in Section 4, Device Processing Results.

The demonstration interconnection scheme shown in **Figure 1** requires that the silicon carry the laterally flowing device current. The sheet resistivity of the base and emitter layers will therefore limit the cell width. For cells greater than 1.0 cm wide conduction must be enhanced to eliminate resistive losses. A deep emitter process can be used to increase emitter conduction. Grids can be added during the metallization step. The base conduction can be assisted by a back plane conductor as discussed in Section 2.1D.

3. Materials Processing Results

3.1 Introduction

An insulating ceramic has been developed that has a resistivity higher than the 500 Ωcm required of the Product III device design. The areal generation capabilities of ceramic substrates have been increased to generate samples greater than 500 cm^2. All ceramics are fabricated in-house at AstroPower and utilize low-cost materials and processing. Ceramic fabrication capabilities were demonstrated by delivering ceramics greater than 500 cm^2 to NREL.

The metallurgical barrier deposition process has been developed to uniformly cover areas over 500 cm^2. The silicon deposition equipment has also been altered to uniformly deposit silicon over areas greater than 400 cm^2. Light trapping structures require one or more surfaces to be textured. Random texturing has been incorporated into the ceramic-metallurgical barrier surface.

An investigation of light trapping on the similar Product II Silicon-Film structure (planar junction, conducting ceramic) indicated high levels of light trapping from similar random texturing [3].

3.2 Morphology and Impurities

Similar to the earlier Product II results [4], films of good morphology have been formed on the insulating Product III ceramics. Grain size is on the order of millimeters and aspect ratios exceed 10 for the 100 μm thick films.

To investigate silicon quality, single junction devices were formed on the insulating substrates with both electrical contacts made to the front of the device. Characterization of small area devices (0.1 cm^2) revealed efficiencies of approximately 7%. Device performance is limited by low diffusion length (<10 μm) resulting in poor short circuit current.

To understand the source of the poor minority carrier properties, chemical analysis of the silicon feedstock was undertaken. Neutron activation analysis was utilized to investigate impurity levels. High levels of Fe (20 ppm), Cr (2 ppm) and Cu (10 ppm) were found. These high levels of impurities could explain the poor minority carrier properties being seen in our samples.

To generate a baseline device result, 1.0 cm^2 devices were fabricated on older, less-pure feedstock. Devices were formed using 200 μm thick Silicon-Film layers on an electrically insulating substrate. Back contact was made by mechanically making access to the silicon through the ceramic and applying aluminum paste. No metallurgical barrier was present. A single layer Si_3N_4 anti-reflection layer was used. The best device results were

$$V_{oc} = 542 \text{ mv}$$
$$J_{sc} = 16.45 \text{ mA/cm}^2$$
$$FF = 70.0$$
$$\eta = 6.24\%$$

A review of in-house material handling procedures was conducted. The chemical analysis of silicon samples representing different points in the handling procedure indicates that improved handling procedures did lower impurity levels to the detection limits of the neutron activation analysis used (approximately 1 ppm for the transition metals). Although an improvement from our initial investigation, significant levels of impurities can still exist to degrade minority carrier properties.

A second source of silicon was identified and acquired with high purity specifications. Test structures were fabricated with

the higher purity material, handled with revised processing procedures. Initial results were positive, with minority carrier diffusion lengths of 30 to 50 μm being measured on all-silicon devices fabricated by the silicon-film process. Plans are in place to incorporate the high purity material in the full silicon-on-ceramic program.

3.3 Phase I Deliverables

The following deliverable samples were sent 11/21/91;

Addressing Task 1:
(2) Low-cost ceramic substrates (both samples are 540 cm^2).
Addressing Task 2 and Task 3:
(2) Low-cost ceramic substrates with metallurgical barrier coating and random surface texturing (both samples are 360 cm^2).
Addressing Task 5:
(2) Low-cost ceramic substrates with metallurgical barrier coating and deposited silicon layer (373 cm^2 and 338 cm^2).

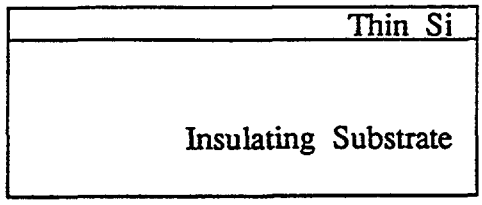
To verify the state of development of the materials programs a set of large area ceramic based samples were sent to NREL on 11/21/91. Included in this set were ceramics samples approximately 540 cm^2 in size. This large area was achieved through process and equipment development at AstroPower. Samples approximately 350 cm^2 demonstrating barrier layers, surface texturing, and deposited silicon layers were also delivered.

4. Device Processing Results

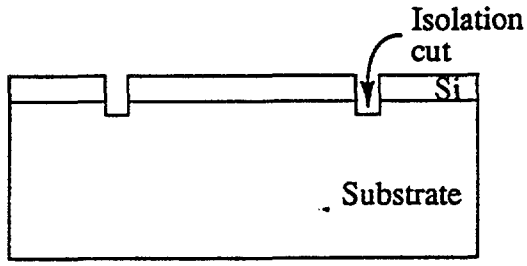
4.1 Introduction

A process sequence was devised early in the program to monolithically interconnect the silicon on ceramic. This early program did not account for the presence of a back plane conductor. The initial process sequence is shown in **Figure 6.**

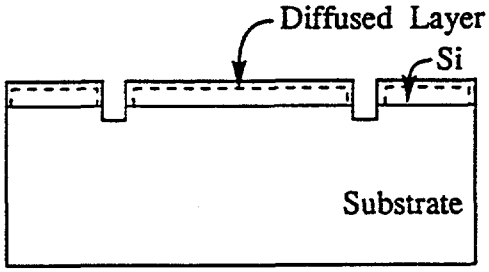
1) Silicon on Ceramic Structure



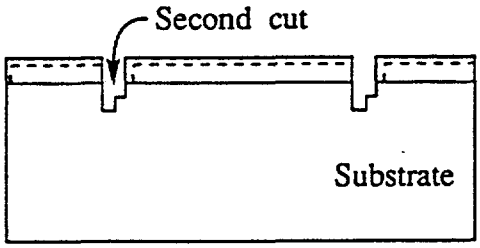
2) Isolation



3) N-Layer Diffusion



4) Re-Isolation



5) Metallization

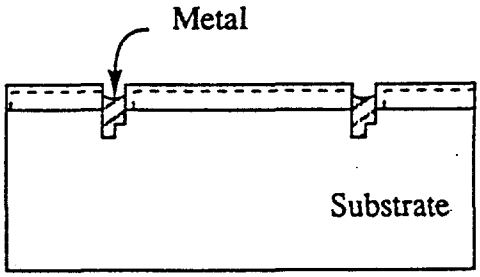


Figure 6. The initial monolithic interconnected solar cell processing sequence.

The Product III process, as shown in **Figure 6(1)** begins with a substrate of p-type silicon on ceramic. A metallurgical barrier may or may not be included. As discussed above, an isolation cut is first made to define cell area (2). A phosphine or $POCl_3$ based diffusion is then performed to create a phosphorus doped n-type layer on the device surface, as well as line the interior of the trenches (3). A second isolation cut is then performed to remove the n-type lining from one side of the trench (4). Finally, the trench is filled with metal to interconnect the n-type region of one cell to the p-type region of the neighbor cell (5). A photograph of an isolated cell is shown in **Figure 7.**

A series of test structures has been fabricated to verify the processing steps. To adequately interconnect isolated cells, a two part metallization system had to be developed. High temperature metallization is used to make ohmic contact to the silicon, and a low temperature metal to fill the trench. The process sequence in **Figure 6** has been further developed to allow for the incorporation of both a back plane conductor and a front grid conductor. Such a process eliminates any series resistance limitation to cell size.

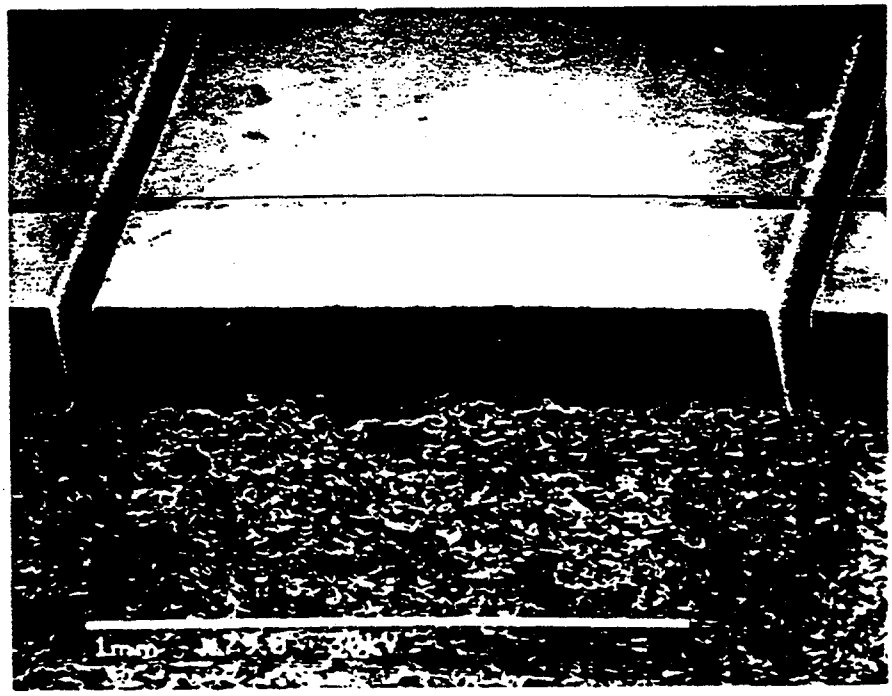


Figure 7. Cross section of silicon on ceramic structure showing isolation trenches (50X magnification).

Solar cells have been fabricated on a regular basis to assess material quality. Impurity problems have been encountered with both in-coming feedstock, and with handling procedures. A second silicon feedstock source has been developed. Handling procedures have been improved to minimize contamination. Recent results indicate that the levels of impurities have been significantly reduced from the baseline level. The baseline level has been shown to generate low diffusion length material with overall conversion efficiencies of 6%.

To demonstrate the process sequence, free-standing silicon wafers were utilized as test structures. A process was developed that supported these wafers on a temporary substrate so that a monolithic processing sequence could be performed. Seventeen isolated cells were interconnected to generate a V_{oc} of 8.25V, measured under AM1.5 illumination. Detailed discussion of the process development has been separated into the following sections on device isolation (trench formation) and metallization.

4.2 Isolation Process (Trench Formation)

A process has been developed that is capable of interconnecting isolated devices on a monolithic substrate. For the critical step of device isolation the processes considered were dicing, laser ablation, and chemical etching. The requirements of the isolation process include the ability to form deep narrow trenches through the silicon and portions of the barrier and ceramic. Dicing was chosen as the best alternative to meet the short term goals. The advantage of dicing is that the equipment is readily available and amenable to a production process. Trenches 50 μm wide and over 100 μm deep were easily obtained. Saws were utilized that could cut both silicon and ceramic. An example of a sawn trench is shown in **Figure 7**. The only disadvantage of dicing is it imposes a strict specification on wafer flatness. The use of a laser to form the trenches would relax the flatness specification, and may be investigated in later work. The investigation of chemical etching is also postponed until silicon active layers are closer to the target thickness of 35 μm, for ease of trench width control.

To demonstrate both the isolating properties of the substrate and the isolation process, a test structure was developed. Samples of Silicon-Film on insulating ceramic were used as the starting material. The thickness of the silicon layer on these devices was approximately 75 μm (3 mils). Samples were subjected to the following process sequence;

1. Al/Ag paste was screen printed and fired to form an ohmic contact to the silicon layer.
2. Deep (20 mil) isolation trenches were cut around a mesa (0.3 mils x 0.2 mils).
3. Sample was tested to insure that the mesa was isolated from surrounding silicon film layer.
4. A shallow cut was made down the center of the mesa, and the resistance between the two sections was tested. Consecutive cuts of increasing depth were made (0.25 mils deeper each cut).

An example of the test data is shown in **Figure 8.** Included in the inset is a schematic of the test structure.

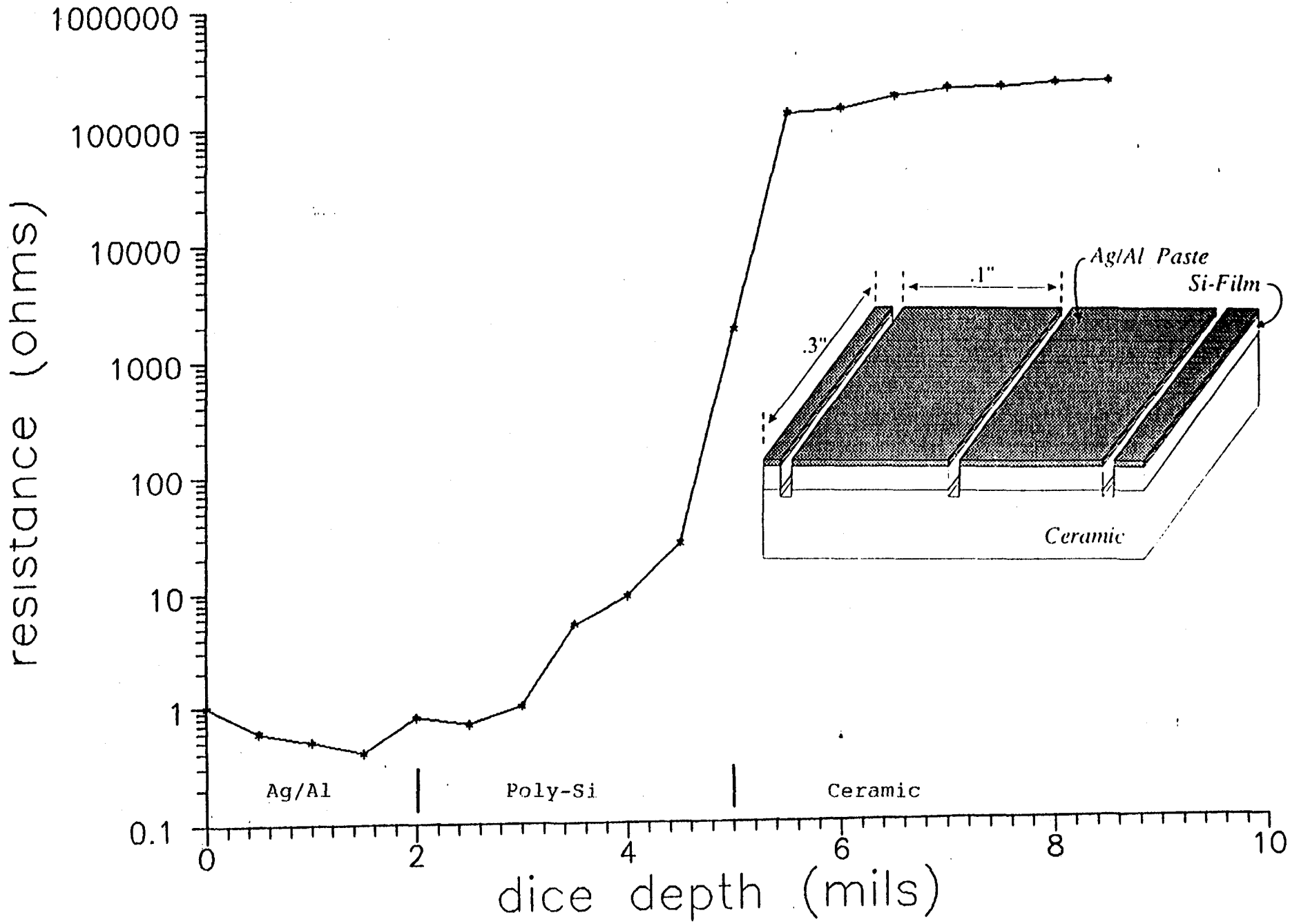


Figure 8. Isolation Test Structure test data. The inset shows a schematic of the device.

As **Figure 8** reveals, when the trench depth exceeded the silicon layer thickness, the resistance increased as expected. The magnitude of the inter-cell resistance increased 4 orders of magnitude as the trench depth increased 25 μm past the layer depth. The results show that the ceramic is sufficiently insulating (>500$\Omega/_{\square}$) to provide good electrical isolation. The boundary between the silicon and ceramic varied +/- 1.0 mil (this sample did not contain a barrier).

4.3 Trench Metallization

The metallization of the trench was initially conceived to be a one-step process, as shown in the process sequence of **Figure 6.** As process development has since shown, material and electrical constraints do not allow this level of simplicity. The different metallization efforts will be discussed in the order they were developed, as well as the processing and materials issues that were discovered.

A process using screen printable aluminum/silver paste was developed and tested on metallization test structures. These contact resistance test structures were fabricated from samples of Silicon-Film on insulating ceramic. Silicon layer thickness was approximately 200 μm. Samples underwent the following process sequence (a schematic of the device structure and a photograph of a metallized trench is shown in **Figure 9**);

1. Silicon on ceramic samples were diffused by a phosphine gas source. The resulting n-type layer had a sheet resistivity of 55-60 $\Omega/_{\square}$ and a junction depth of approximately 0.3 microns.

2. Deep (250 μm) isolation trenches were cut to form 7 isolated cells. Each cell measured 1.9 mm by 8.6 mm. Isolation trenches were 50 μm wide.

3. Al/Ag paste was squeegeed into the trenches with a screen printing apparatus (no mask was used). The paste was then carefully washed from non-trench areas.

4. The samples were then fired in a IR belt furnace.

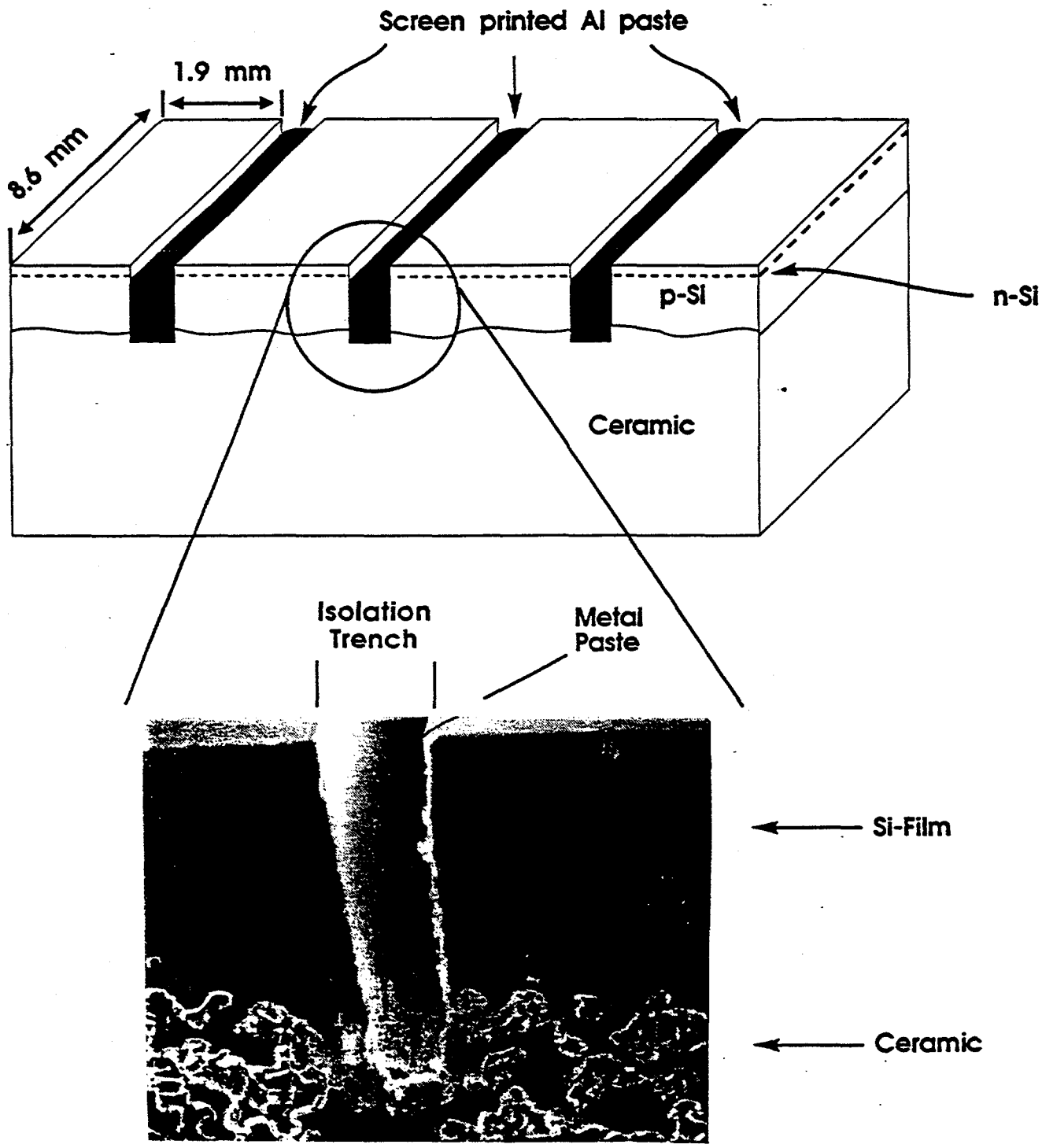


Figure 9. Contact resistance test structure with trench lined with metal paste.

The contact resistance test structures were tested for resistance between consecutive parallel trenches. The experimentally measured resistance data is shown in **Figure 10**. The resulting best fit line is

$$y=5.38\Omega(n)+3.58\Omega$$

Fitting the data to the equation

$$R=\rho\frac{L}{A}(n)+2R_c$$

results in

$$R_c=1.79\Omega$$

$$\rho=(\frac{A}{L})5.38\Omega=0.5\Omega cm$$

The experimentally measured value was 30% lower than the base layer resistivity of 0.8 Ω-cm. This was initially believed to be due to the shorting of the emitter to the metal paste. Further evaluation discovered that a high conductivity layer was being formed during the silicon deposition step between the ceramic and the Silicon-Film layer (the samples used for these test structures are formed without a barrier). This situation is schematically shown in **Figure 11**. The high conductance layer is believed to be due to impurities from the ceramic interacting with the initial few microns of deposited silicon. This high conductance layer will be eliminated by the use of the metallurgical barrier.

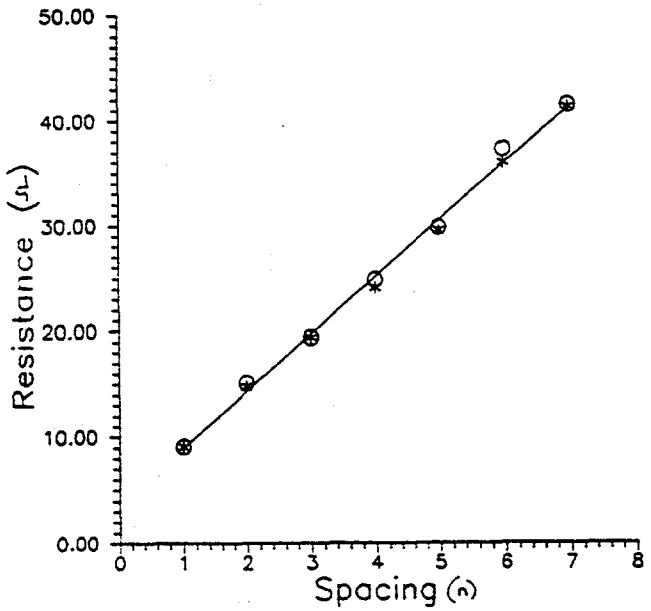


Figure 10. Contact resistance test data.

An important element of the full monolithic device design is the incorporation of a low conductance back plane to minimize Rs effects, as discussed in Section 2.4. The present shunting problem caused by the high conduction ceramic-silicon interface was considered worth solving. If a process could be devised that alleviated the detrimental effects of this layer, such a process could accept the intentional back conductor plane intended for later development. A revised process was therefore developed that is unaffected by the presence of a high conduction back plane. That process sequence is shown in **Figure 12**.

The new process (as well as the previous process) utilizes only one metallization step. That metal system must contact both n and p type silicon. Although the Al/Ag paste, used in the initial experiments, was found to be successful at contacting p-type material, no Al/Ag combinations were found that could contact both n and p-type material. All pastes containing even trace amounts of aluminum caused emitter junction shorting (through aluminum/silicon alloy formation and spiking). Silver-only pastes were found to contact the highly doped n-type surface easily, however an adequate process window for the p-type contact was not found. In addition to Al and Ag, other low temperature metals such as In and Sn were evaluated with limited success.

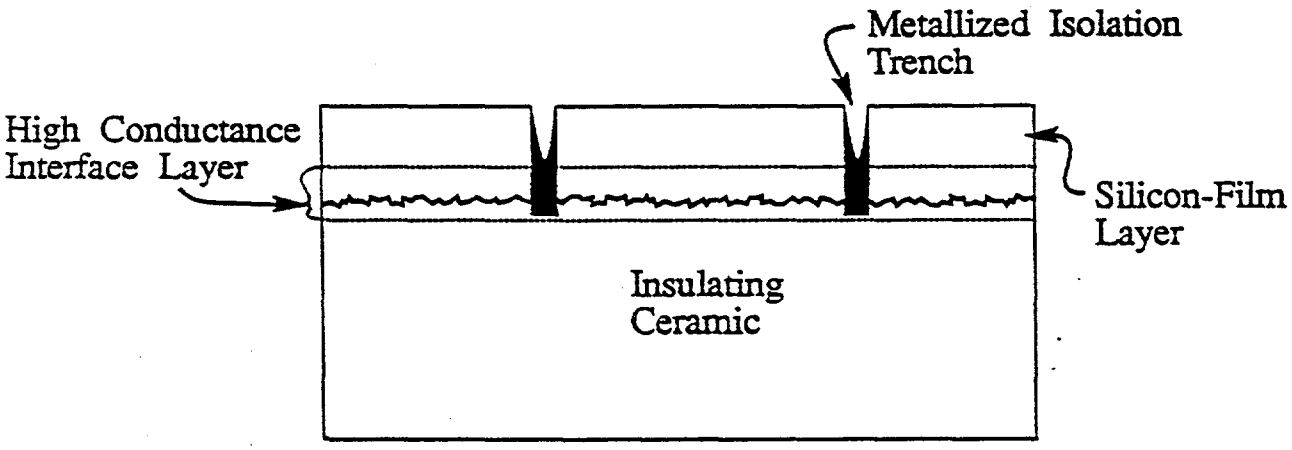
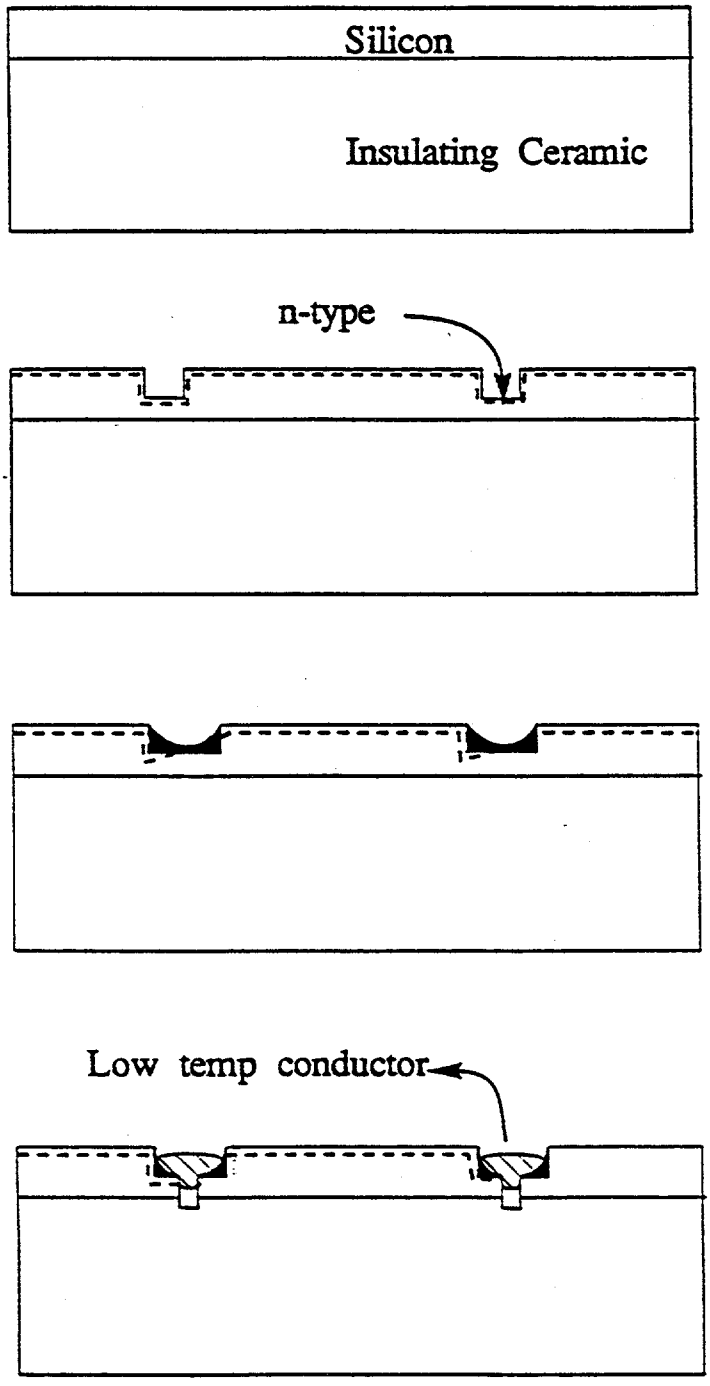


Figure 11. Schematic of the Product III device, showing high conduction Silicon-Film/ceramic interface layer.

A nickel plating process, presently in use for plating laser grooved buried contact solar cells was found to perform well. The electro-less plating process offers the further benefit of being low cost and production oriented. A process window was established that makes low resistance ohmic contact to both n and p type material, without emitter junction shunting.



Silicon on ceramic starting material

1. dice metallization trench
2. Phosphorus diffusion
3. second isolation step
4. metallization
5. Final isolation
6. low temp interconnect

Figure 12. Revised process sequence developed to accept a conducting back plane at the silicon/ ceramic interface.

5. Single Crystal Test Structures

The process sequence shown in **Figure 12** has been exercised on free standing silicon wafers (single crystal and large grain polycrystalline). This effort was pursued to develop the needed process steps in a timely manner and establish proof of concept. The process sequence in **Figure 12** was altered slightly to work with conventional thick silicon wafers. Changes were required in the final two steps. The final isolation step (originally a diced trench through the silicon layer into the ceramic) is altered to be a diced trench completely through the all-silicon wafer. The last process step, the application of low temperature metal, must be capable of holding the diced sections together as well as acting as the electrical contact. Significant effort was required to develop a system that would penetrate the diced isolation trenches, make electrical contact to the previously metallized device contacts, and adhere well.

The process has been demonstrated on large grain cast polycrystalline wafers. A 25 cm^2 wafer was fabricated into 17 interconnected cells. Each cell was 1.47 cm^2. The measured V_{oc} under AM1.5 illumination was 8.25 volts. This corresponds to an average V_{oc} of 485 mV per cell. High levels of series resistance made the fill factor and overall efficiency low. An investigation into the causes of the high series resistance is underway.

This test sequence has demonstrated the production-based monolithic process. The process has been shown to be viable and capable of maintaining reasonable open circuit voltages over a 17 cell string. The use of test structures is continuing in order to optimize all the metallization steps for low R_s and high efficiency.

6. Conclusions

Critical elements of the monolithically integrated device have been developed. An insulating ceramic substrate has been developed and tested. Ceramic areal generation capabilities have been expanded to 500 cm^2. A monolithic interconnection process has been developed that will isolate and interconnect individual cells on the ceramic surface. Production based, low cost process steps are utilized. The process was verified using free-standing silicon wafers to achieve a V_{oc} of 8.25 volts over a 17 element string. Overall efficiency of the Silicon-Film material has been limited to 6% due to impurities. Improved processing and feedstock materials are under investigation.

7. References

[1] M.L.Rock, D.W.Cunningham, C.L.Kendall, R.B.Hall, A.M.Barnett, "Process Induced Improvements in Polycrystalline Silicon-Film Cells", Proceedings of the 21st IEEE PVSC, Orlando, Florida, May 1990, pp. 634-637.

[2] A.M. Barnett, 5th International PV Science and Engineering Conference, November 1990, Kyoto, Japan, pp. 713-718.

[3] J.A. Rand and P.A. Basore, "Light-Trapping Silicon Solar Cells, Experimental Results and Analysis", presented at the 22nd IEEE Photovoltaics Specialists Conference, Las Vegas, Nevada, October 1991.

[4] J.A.Rand, D.H.Ford, C.Bacon, A.E.Ingram, T.R.Ruffins, R.B.Hall, A.M.Barnett, "Silicon-Film Product II: Initial Light Trapping Results," Proceedings of the 10th European Photovoltaic Science and Engineering Conference, April 1991, pp. 306-309.

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16. Abstract (Limit: 200 words)

This report describes work to develop Silicon-Film Product III into a low-cost, stable device for large-scale terrestrial power applications. The Product III structure is a thin (< 100 μm) polycrystalline silicon layer on a non-conductive supporting ceramic substrate. The presence of the substrate allows cells to be isolated and interconnected monolithically in various series/parellel configurations. The long-term goal for the product is efficiencies over 18% on areas greater than 1200 cm^2. The high efficiency is made possible through the benefits of using polycrystalline thin silicon incorporated into a light-trapping structure with a passivated back surface. Short-term goals focused on the development of large-area ceramics, a monolithic interconnection process, and 100 cm^2 solar cells. Critical elements of the monolithically integrated device were developed, and an insulating ceramic substrate was developed and tested. A monolithic interconnection process was developed that will isolate and interconnect individual cells on the ceramic surface. Production-based, low-cost process steps were used, and the process was verified using free-standing silicon wafers to achieve an open-circuit voltage (V_{oc}) of 8.25 V over a 17-element string. The overall efficiency of the silicon-film materials was limited to 6% by impurities. Improved processing and feedstock materials are under investigation.

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