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ABSTRACT

In this paper, we have focused on the formation and the role of CdS/CdTe interface on CdTe solar cells. The devices were made using chemical bath deposited (CBD) CdS on SnO_2/glass substrates and the CdTe was deposited by close spaced sublimation (CSS). CdTe was treated with $CdCl_2$: known to be a key processing parameter. Compositional analysis showed considerable interdiffusion of Te and S as well as Cl accumulation at the interface. Micro-photoluminescence (PL) analysis reveals sulfur accumulation at the grain boundaries and a graded CdSxTe1-x alloy at the interface. Our analysis leads us to conclude that Cl accumulation and anion vacancies result in a one sided n^+-p junction. This model could explain the collection loss in the CdS layer, seen in the spectral response of CdS/CdTe devices.

INTRODUCTION

CdS/CdTe solar cells have demonstrated efficiencies of 15.8% [1]. Due to its good stability and ease of fabrication, a number of groups are involved in development of this technology. There however are many issues that still need to be understood for successful commercialization. The CdS/CdTe interface plays an active and a detailed knowledge of its properties is crucial for thorough understanding of the device. High efficiency devices have been obtained in spite of the large lattice mismatch (9.7%) between hexagonal CdS and cubic CdTe. Interdiffusion at the CdS/CdTe interface is considered to affect the performance of the devices. CdCl2 heat treatment is a key step in CdTe device processing. Roh and Im [2] reported that, for screen printed cells, the spectral response of the devices showed heterojunction behavior for lower quantities of $CdCl_2$ and the efficiency increased with $CdCl_2$ concentration. For higher concentration of $CdCl_2$, the devices had behavior characteristics similar to buried homojunction with the depth of the buried homojunction, increasing with the concentration of $CdCl_2$. They attributed this behavior to enhanced interdiffusion of CdS and CdTe at the interface. Several authors [3] have reported on the effect of interdiffusion on device properties. The effect of grain boundaries and other structural defects on the device properties is not fully understood. In this paper, we report on the interdiffusion at CdS/CdTe interface for CBD-CdS/CSS-CdTe structures deposited at different temperatures before and after $CdCl_2$ heat treatment. Structural defects and phases present at the interface are investigated by transmission electron microscopy (TEM). The effect of grain boundaries and structural defects on electro-optical properties is studied by micro-photoluminescence (PL) measurements. Device modeling results, based on interface characterization data, are presented to explain the lack of carrier collection in the CdS layer.

EXPERIMENTAL DETAILS

CdS films, ranging from 80 to 100 nm in thickness, were grown on glass/SnO_2 substrates by CBD. The CdTe films were deposited using the CSS technique in a He/O_2 mixture with a total reactor pressure of 15-30 torr at substrate temperatures of 500°-600°C. CdTe films with thicknesses of 0.5 μm to 10 μm were used. Post-deposition $CdCl_2$ heat-treatment was carried out by dipping the samples in a 50% saturated solution of $CdCl_2$ in methanol at 55°C, followed by annealing at 400°C in a 4:1 volume ratio He/O_2 ambient for 30 min. Samples were then etched using a nitric acid : phosphoric acid : water etchant. Graphite:HgTe based back contacts were applied to complete the devices.

Si/CdS/CdTe structures were used for TEM analysis. SIMS analysis was performed on a Cameca IMs-3f with a Cs^+ primary ion beam, and detection of negative secondary ions. TEM analysis was carried out using a Philips CM-30 microscope operating at 300 kV. For the micro-PL measurements, the sample was mounted on a cold finger of an Oxford Microstat helium cryostat held at 4.2 K, and the 5145 Å line of an Ar ion laser was used as the excitation source. An incident power of about 50 mW of the laser was focused using an all-mirror microscope objective (N.A.=0.5) onto the sample. The focus spot was scanned by moving the sample stage (with the cryostat) with a high-resolution translation stage. The PL signal was collected by the same objective, dispersed by a SPEX 1877 0.6-m triple spectrometer, and detected with a high-resolution CCD array. The spatial resolution determined by the size of the laser spot was about 2 μm.

RESULTS

SIMS depth profiling was used to determine the extent of interdiffusion at the CdS/CdTe interface as a function of substrate temperature and post-deposition $CdCl_2$ heat treatment. SIMS analysis on the CdTe films deposited at different temperatures showed that CdTe surface roughness limits compositional resolution to approximately the root mean square (RMS) of the surface roughness. Atomic Force Microscopy analysis showed that the RMS surface roughness ranges from 100 nm for 500°C films to 550 nm for 600°C films. To minimize the problem of surface roughness, the samples were polished to approximately 5 nm.

SIMS compositional profiles for a polished sample deposited at 550°C, before and after $CdCl_2$ treatment, are shown in Fig. 1. Data for a sample deposited at 600°C are shown in Fig. 2.

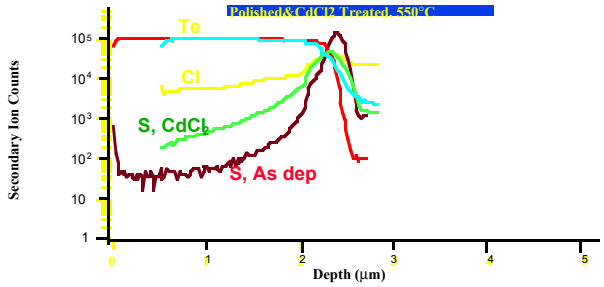

Fig. 1. SIMS depth profile for polished sample deposited at 550°C before and after $CdCl_2$ treatment.

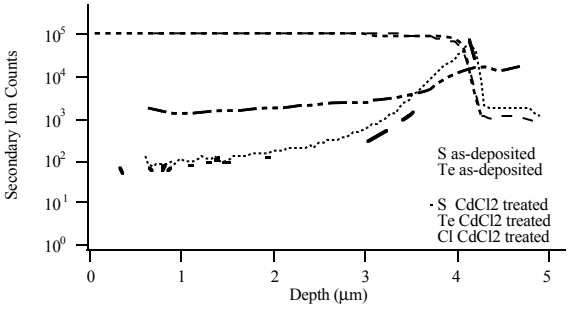

Fig. 2. SIMS depth profile for polished sample deposited at 600°C before and after $CdCl_2$ treatment.

For untreated samples deposited at 550°C, the intermixing at the interface is minimal. For samples deposited at 500°C, the interface is almost abrupt. We find that $CdCl_2$ heat treatment promotes considerable interdiffusion at the interface for samples deposited at these lower substrate temperatures. For untreated samples deposited at 600°C, there is considerable sulfur diffusion into the CdTe and the profile changes only slightly after $CdCl_2$ heat treatment. After $CdCl_2$ treatment, for samples deposited at all temperatures, there is considerable chlorine accumulation at the CdS/CdTe interface. The amount of chlorine in the bulk CdTe, away from the interface, is higher for samples deposited at lower temperatures. AFM measurements showed that there was no CdTe grain growth, for samples deposited at different substrate temperatures, after $CdCl_2$ heat-treatment.

Based on these results, it appears that during $CdCl_2$ heat-treatment, $CdCl_2$ penetrates along the grain boundaries and there is accumulation of $CdCl_2$ at CdS/CdTe interface. Samples deposited at lower temperatures have smaller grains and consequently higher grain boundary volume. This would explain the higher levels of chlorine seen in these samples.

Auger electron spectroscopy (AES) analysis showed that the extent of interdiffusion at the interface was up to 500 nm depending on the processing parameters[4]. Both AES and SIMS analysis reveal that the interdiffusion is one-sided, i.e. there is more sulfur diffusing into the CdTe than Te diffused into the CdS. Even though the thickness of the CdS layer is only 100 nm, AES depth profiles show negligible Te through bulk of the CdS layer (<0.1 at.%). SIMS depth profiling shows that Te diffusion into CdS is limited mainly to the surface layer and the bulk of the CdS layer does not contain much Te.

Cross-sectional TEM analysis was performed on Si/CBD CdS/CSS CdTe structures. Si substrates were used to facilitate sample preparation. The purpose of this analysis is to study the growth morphology of both CdS and CdTe as well as to investigate the structural and chemical properties of the CdS/CdTe interface region. While the deposition conditions of the CBD CdS were kept constant, three different deposition temperatures (425, 525, and 625°C) were used for CdTe. The CdS films exhibited a very fine-grain morphology with some amorphous characteristics and a tendency to a preferred orientation. Furthermore, the grains are heavily faulted with a high density of stacking faults and micro-twins. This is a significant finding as our work on the generation and propagation of defects in CdTe films showed that planar defects in the underlying CdS tend to propagate across the CdS/CdTe interface. TEM studies also showed that CdS has a predominantly hexagonal lattice in both as-deposited and heat-treated forms.

The morphology of CdTe films deposited at lower temperatures appeared markedly different from those deposited at high temperatures. At 425°C, small CdTe grains were observed near the interface. The grain size, however, increased significantly as the film thickness increased. The 625°C sample, on the other hand, exhibited columnar growth in CdTe and little increase in grain size was observed across the thickness of the film. Detailed cross-sectional TEM examinations were performed on as-deposited CdTe films. The films were found to be heavily faulted with a high density of planar defects and threading dislocations. Fig. 3 is a TEM cross-section of a typical Si/CdS/CdTe structure. The CdTe film was deposited at 525°C. This figure clearly shows the high density and

the three-dimensional distribution of planar defects. These defects are primarily stacking faults and micro-twins on {111} planes. Their density, however, varies considerably from one grain to another.

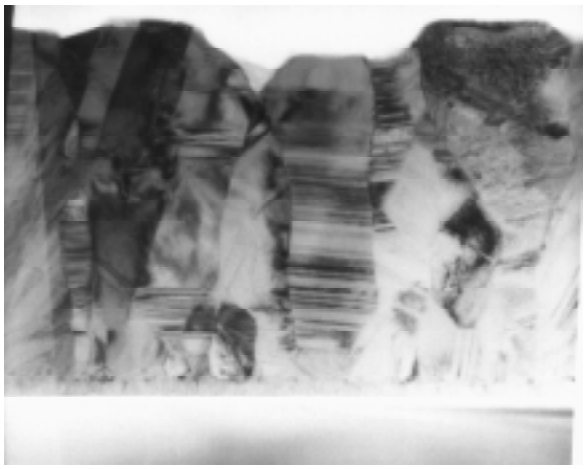

Fig. 3- TEM cross-section of a typical Si/CBD CdS/CSS CdTe deposited at 525°C

Compositional analysis by small-area, energy-dispersive x-ray analysis (EDS) revealed significant sulfur diffusion into the CdTe film. The amount of sulfur was below detection limit (<0.1 at.%) at the lowest deposition temperature, and increased with increasing deposition temperature. Furthermore, significantly higher amounts of sulfur were detected both at the grain boundaries and within heavily faulted grains (as opposed to the grains with minimum defect density).

Fig. 4 shows PL intensity as a function of position from a film that was released from the substrate directly exposing the CdS/CdTe interface. The sample was deposited at 610°C and the $CdCl_2$ heat treatment was used. The peaks correspond to the center of the grains, and the valleys to the grain boundaries in the material. This correlates well with the grain sizes seen in the TEM micrograph shown in Fig. 3. The points between 30 and 35 μm, and 49 and 51 μm, correspond to small grains ~ 2-3 μm wide. PL intensity analysis from the CdTe side also shows similar behavior. PL spectra measured from the CdTe side and the CdS/CdTe interface side (for selected points in Fig. 4) are presented in Fig. 5. The PL spectra for measurements on the CdTe side show that, even though the intensity changes considerably from the center of the grain to the grain boundary, the peak position of the spectra remains at the same position (1.579 eV), corresponding to the CdTe bandgap. On the other hand, the PL spectra from the CdS/CdTe side show changes both in the intensity and the peak position. All of these spectra are

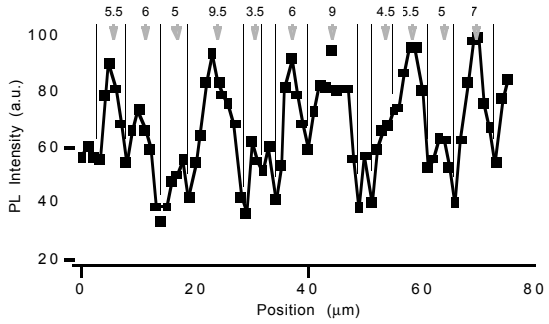

Fig. 4. PL Intensity vs position for measurements from CdS/CdTe side.

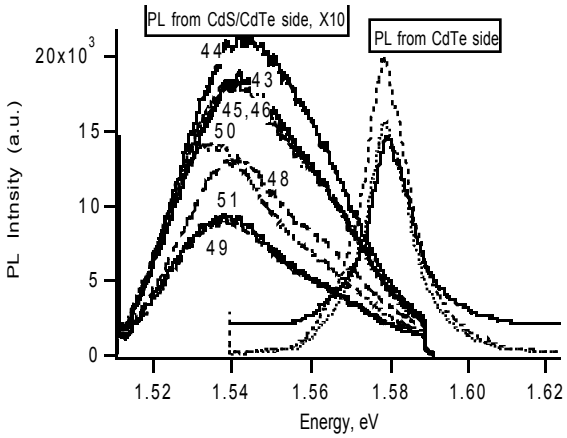

Fig. 5. PL spectra measured at 4.2°K from the CdTe and the CdS/CdTe side. The numbers refer to the position in Fig. 4.

shifted to lower energy and their bandwidth is much larger than that of the CdTe spectra seen from the backside. These spectra correspond to the alloyed region at the interface, which explains the peak shift to lower energies (expected for Te-rich CdS_xTe_{1-x} alloys) [5]. Peak-broadening is due to the superposition of spectra corresponding to the range of alloy compositions present in the alloyed layer. The spectra corresponding to the positions in the center of the large grain (~9 μm) have higher intensities, with a peak position at 1.543 eV and symmetrical peak broadening, suggesting alloy compositions in the range of 1.524 eV and 1.569 eV. The spectra corresponding to the center position of a small grain (~2 μm) has a peak position at 1.535 eV and is asymmetrical, indicating the contribution predominantly from the lower gap alloys between 1.52 eV and 1.545 eV. The peaks corresponding to the grain boundaries (lowest intensity peaks in the spectrum) have peak positions at 1.538 eV, and also show predominant contribution from lower gap alloys. Previous work on Te-rich CdS_xTe_{1-x} alloys [5], indicates that the bandgap decreases as x

increases from 0 to 0.25. Therefore, grain boundaries and heavily faulted small grains contain alloys with higher sulfur compositions as compared to the middle of the larger grains. This is the result of higher sulfur diffusion along grain boundaries and planar faults as seen from micro-EDS analysis of TEM samples.

Device modeling was done using SIMS-Windows software [6]. Fig. 6 shows the schematic of the device used for modeling. CdS films deposited by CBD have resistivities in the range of 10^4-10^6 Ω-cm. Based on these high resistivities, we have assumed a CdS carrier concentration of 10^{14} cm^{-3}. The electric field for this case is shown in Fig. 7 (denoted by Nd = 1e14). The hole concentration for CdTe was assumed to be 10^{15} cm^{-3}.

Fig. 6. Schematic of the device.

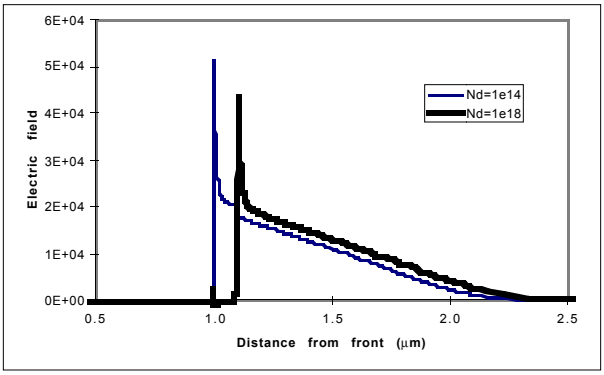

Fig. 7. Electric field calculated using Simwindows for N_d = $1x10^{14}$ cm^{-3} and $1x10^{18}$ cm^{-3}

We have also assumed that the bands line up at the interface, as a result of intermixing at the CdS/CdTe interface. Fig. 7 shows that there is an electric field present throughout CdS layer, terminating at the surface of SnO_2 layer. The CdS in this case is similar to the i-layer in an a-Si device, and thus one would expect considerable carrier collection due to photons absorbed in the CdS layer. However, in CdTe devices, quantum efficiency measurements indicate poor collection of carriers generated in the CdS. Therefore this device model does not adequately explain device performance. If this band diagram were correct, there should be some field assisted collection despite the poor electronic quality of the CdS layer.

The SIMS results discussed earlier suggest an alternative band-diagram that explains the device performance better. Chlorine is a known n-type dopant in both CdS and CdTe. Thus the chlorine accumulated at the CdS/CdTe interface can dope the CdS creating a n^+-layer. There is also considerable diffusion of sulfur into CdTe. This can create anion vacancies in the CdS which can also lead to n-type doping. The modeling results with a n^+ layer at the interface with an assumed carrier concentration of 10^{18} is presented in Fig. 7 (denoted by Nd= 1 e 18).

With this model the space charge region terminates close to the CdS/CdTe interface leaving part of the CdS without any electric field. This could explain the lack of current collection in the CdS layer (assuming only field assisted current collection on the CdS side). CdS has fairly small grains (~30-50 nm) and TEM analysis showed that the grains are heavily faulted with a high density of stacking faults and microtwins. These factors would reduce the mobilities in the CdS. The lifetimes in as-deposited CdS were measured by TRPL to be ~ 200 ps. During device processing, there is diffusion of Te into the CdS. Te concentrations as low as 10^{17} cm^{-3} are known to create midgap levels in CdS thereby reducing the lifetime [7]. A lifetime of 20 ps and a mobility of 1 cm^2/V-s yields a diffusion length of 32 Å. Therefore, the assumption of only field assisted collection would be valid.

CONCLUSIONS

Compositional, structural and electro-optical analysis of CdS/CdTe interface shows that the properties of the interface have a significant effect on the device properties. A device model based on this analysis satisfactorily explains some of the key device properties.

ACKNOWLEDGMENTS

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