



# Empirical Evaluation of GPS Clock Accuracy for Isochronous Droop-Based Inverters

## Preprint

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*National Renewable Energy Laboratory*

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# Empirical Evaluation of GPS Clock Accuracy for Isochronous Droop-based Inverters

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**Abstract**—Grid-forming inverters rely upon an internal reference to regulate the grid’s voltage and frequency. Without a reliable reference, issues such as loss of synchronism, frequency instability, and unequal power sharing can occur. One proposed internal phase reference for grid-forming inverters is generated by the controller’s clock, but this is affected by nonidealities in the crystal oscillator leading to time drift in the phase reference. To improve the controller’s clock accuracy, the Global Positioning System (GPS) can be used to calibrate the internal clock. Previously, GPS-based clock calibration was explored theoretically and various methods were developed for mitigating frequency/phase drift at the power system level. This paper experimentally validates the direct performance of GPS time-calibration at the controller level and justifies its use in maintaining an accurate phase reference for droop-based grid-forming inverters.

**Index Terms**—grid forming inverter, synchronization, GPS, clock drift, droop, stability, power sharing, decentralized

## I. INTRODUCTION

With increasing amounts of Distributed Energy Resources (DER) being connected to the grid and integrated in microgrids through inverters, the need for alternative methods of voltage and frequency regulation is growing. Today, the majority of inverters are grid-following inverters (GFLIs) where the voltage and frequency reference are derived from the interconnected grid, posing the problem of cascading instability for high-penetration feeders and weak grids. To overcome this, grid-forming inverters (GFMI) set their own phase (Fig. 1) and voltage references internally. One popular grid-forming control method is angle droop (1)-(2) which increases/decreases voltage and phase offsets to share power and regulate frequency, however, an invariant phase reference is required to prevent instability from rapid frequency fluctuations and unequal power sharing among converters [1].

$$\theta = \theta_0 - nP \quad (1)$$

$$V = V_0 - mQ \quad (2)$$

The microcontroller’s generated phase reference is dependent upon the accuracy of its internal crystal oscillation circuit which is affected by time drift due to crystal nonidealities. For the many off-grid standalone voltage source inverters using the inverter’s crystal as a phase reference, there are no problems

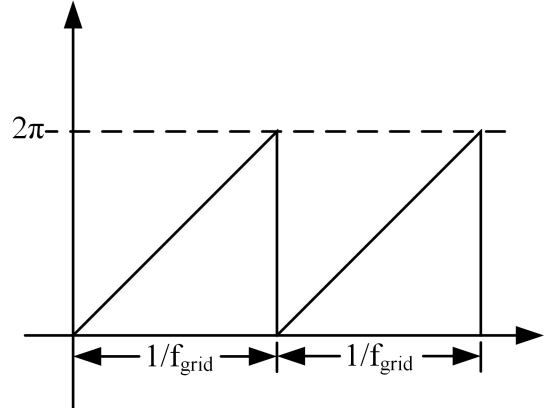


Fig. 1. Ideal Phase Reference Waveform.

since the off-grid inverter is a sole generation source. But for grid-connected inverters, the crystal’s accumulated error over time can lead to the converter solely relying upon droop, potentially causing circulating currents between paralleled inverters and a greater chance of frequency instability [2].

One specific solution to the problem of clock drift causing steady-state error is to add in error-correction terms to the droop equations, as was demonstrated for microgrid applications in [1]. While this is a valid solution to solve the steady-state errors faced by droop controllers, a better solution involves looking at the cause rather than effects of time drift. Another method to directly improve the clock’s accuracy is through adoption of Precision Time Protocol (PTP) [3]. PTP is a method to synchronize clocks across a system while accounting for phenomena such as latency. Unfortunately, PTP works best for inverters within direct proximity as they must be connected via networking wire for optimal performance which is not always possible nor cost-effective with distributed and decentralized inverters.

The clock-calibration method analyzed in this paper utilizes satellites’ atomic clocks through the Global Positioning System (GPS) to calibrate the inverter’s internal crystal at a regular interval using the one pulse. With the ubiquity of smartphones, GPS chips have become small and inexpensive making the technology practical to integrate in GFMI separated over a geographic distance. Additionally, the integration of GPS

allows additional inverter functionality such as GPS-based microsynchronphasors [4] and GPS location-based advanced solar tracking [5] in addition to being an entirely decentralized calibration method. Use of GPS with GFMI is not novel, a good description on the fundamentals of GPS time-calibration as well as a method to handle the loss of GPS signal with an adaptive Q-f controller is presented in [6]. Further, [7] built upon [6] by developing a hierarchical framework with GPS-calibrated converters for GFMI.

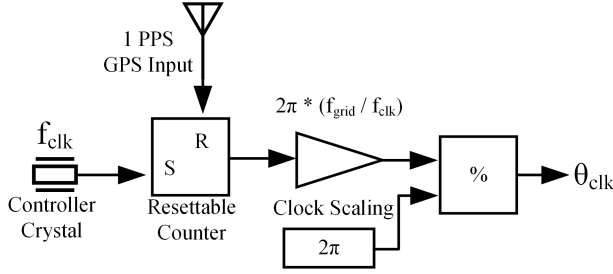


Fig. 2. GPS-calibrated Phase Reference Generator.

For this publication, a generic GFMI is assumed as shown in Fig. 3 to better focus on the phase reference stage as done in [8]. Additionally, a GPS phase reference generator (Fig. 2), which is the foundational piece of a phase generator, is validated in both simulation and hardware.

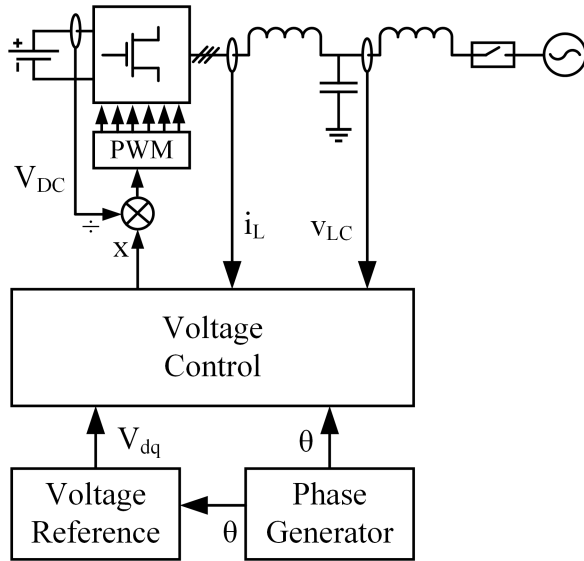


Fig. 3. Generic Grid-Forming Inverter with Phase Reference Stage.

The purpose of this paper is to experimentally validate the performance of GPS time-calibration in maintaining an accurate phase reference for GFMI at the controller level to better justify time-calibration and advanced droop methods. This paper is organized as follows: First, an assessment of possible microcontroller clock drift is conducted to determine the theoretical impact of crystal oscillator error. Next, a model is simulated to validate the theoretical results. Then, a hardware experiment is conducted to experimentally obtain

the actual time drift with and without GPS-calibration. Finally, results are compared and summarized.

## II. CLOCK TIME DRIFT ANALYSIS

Fundamentally, several options exist for a microcontroller's clock source including internal and external sources with one accurate and popular option being crystal CMOS. The ultimate goal of any oscillator is maintaining its exact frequency over periods of time measured as frequency stability in parts per million (PPM). (3) shows how the frequency stability in PPM relates to the nominal frequency difference ( $\Delta f$ ) in Hertz as a function of the carrier frequency ( $f_c$ ) also in Hertz.

$$\Delta f = f_c \frac{PPM}{10^6} \quad (3)$$

Specifically for the TI F28379D Control Card [9], the quartz crystal used is the 20 MHz TXC 7B [10]. This crystal has a factory tolerance of  $\pm 10$  PPM, a temperature variance up to 10 PPM from  $-20^\circ\text{C}$  to  $70^\circ\text{C}$ , and a maximum aging of  $\pm 3$  PPM/year (at  $25^\circ\text{C}$ ). Considering only the factory tolerance of 10 PPM, (3) determines 10 PPM corresponds to a 200 Hz difference for a 20 MHz crystal.

The simplest method to convert clock output into phase output is shown in Fig. 4 and represented by (4).

$$\theta = 2\pi \left( \frac{f_{grid}}{f_{clock}} \text{counter} \right) \% 2\pi \quad (4)$$

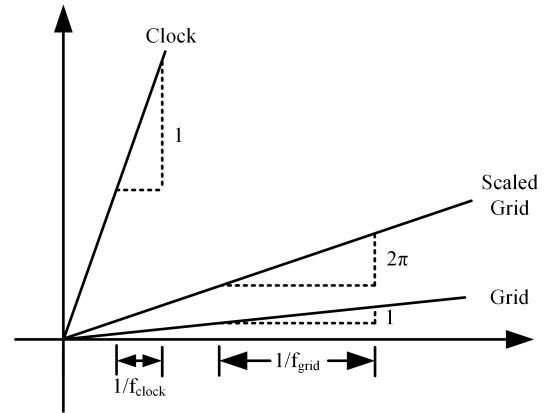


Fig. 4. Clock Slope Conversions.

As an example, a counter running at a nominal 20 MHz over 1 minute (60 seconds) would be valued at  $1,200 \times 10^6$  which, when used with (4), yields  $\theta = 0$  radians as expected. However, if the factory tolerance of +10 PPM (200 Hz) is considered, then the clock's frequency would be 20 MHz + 200 Hz and the total counter value over 1 minute would be  $1,200.012 \times 10^6$  yielding  $\theta = 0.226$  radians ( $12.96^\circ$ ). Assuming the 10 PPM frequency variance is constant, the time drift would steadily increase at  $12.96^\circ$  per minute. By this calculation, the need for GPS time discipline is apparent in maintaining a solid, invariant time reference. Should GPS be lost, an adaptive Q-f phase generator can be used temporarily to ensure an invariant reference until GPS is restored as presented in [6].

### III. SIMULATION SETUP

To determine the impact of a +10 PPM crystal drift, a simple dual GFMI setup was modeled using Simulink as shown in Fig. 5. For a more realistic simulation, line impedances were inserted between each inverter's three-phase output terminal and their shared load bus to represent a typical 120 V line. The specific simulation parameters used are shown in Table I.

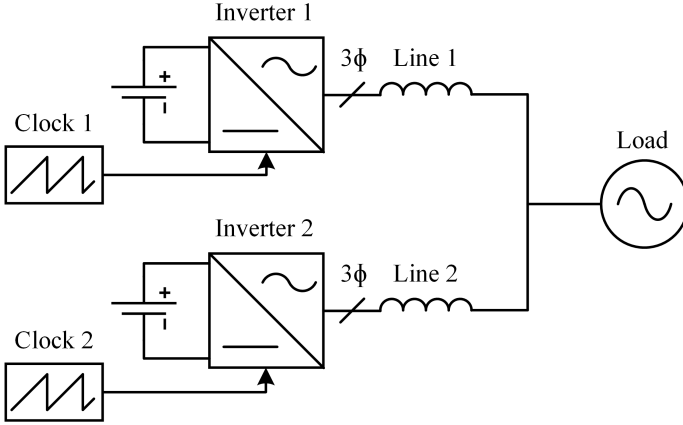


Fig. 5. Dual Grid-Forming Inverter Model with Separate Internal Phase References

TABLE I  
SIMULINK SIMULATION PARAMETERS

Parameter	Value
Line Resistance	154 $m\Omega$
Line Inductance	500 $\mu H$
Angle Droop Constant (n)	0.1
Voltage Droop Constant (m)	0.02
Total Load Real Power	7.5 kW
Total Load Reactive Power	0.6 kVAR
Nominal Line Voltage	120 V

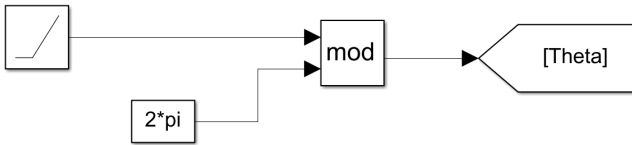


Fig. 6. Ideal Phase Reference Waveform.

With regard to the modeled clocks, two cases are considered: (1) both clocks are GPS-synchronized without drift, (2) one clock is GPS-synchronized and the other has a +10 PPM drift. To accomplish this, the Simulink model of Fig. 6 was used to create a theoretical GPS-disciplined phase generator where only drift is considered. For the case of a time-disciplined phase generator, the ramp's slope is set to  $2\pi * 60$  while the clock with a +10 PPM drift has its slope

set to  $2\pi * 60.0006$  per (5) where GPS-synchronization has a  $\Delta f = 0$  and non-synchronized has a  $\Delta f = 200$  as previously calculated.

$$slope_{uncalibrated} = 2\pi \left( \frac{f_c + \Delta f}{f_c} f_{grid} \right) \quad (5)$$

### IV. SIMULATION RESULTS

Using the two clock cases previously mentioned (with and without GPS-synchronization), several key plots were rendered to determine the extent of power-sharing inequality. Specifically, a clock comparison, real power comparison, and reactive power comparison were plotted for both cases. Case 1 where both clocks are GPS-synchronized yielded Fig. 8 - 10 while case 2 yielded Fig. 11 - 13.

As can be seen from Fig. 12 and 13, as the clock drift (here shown as difference from the GPS-synchronized clock to unsynchronized clock) increases, the unsynchronized inverter progressively takes on more load than the synchronized inverter until the synchronized inverter begins to store power (i.e. battery storage) up through the set power limit which, in this simulation, is infinite. In practicality, the unsynchronized inverter would either be current-limited by internal circuitry or trip offline upon hitting its rating which would require fast power ramping from the synchronized inverter to meet the required load. Unfortunately, this event would likely cause large frequency variation from the load-gen imbalance and potentially trip the load or generation offline. In the case of both inverters having a synchronized clock, it is seen from Fig. 9 and 10 that there is equal power-sharing between the inverters.

### V. EXPERIMENTAL SETUP

To minimize discrepancies between simulation and hardware implementation, the Simulink C2000 Embedded Coder was used to convert the simulated model into hardware. Specifically, the modeled phase generator (Fig. 6) was modified to yield a basic GPS time-discipline phase generator as in Fig. 7. From left to right, first a GPIO (General Purpose Input Output) block is used to obtain a logical true from a connected GPS time base. This value is buffered and adjusted to internal sampling rate before being fed into a resettable counter which increments on each system clock tick but resets upon receiving a logical true from GPS input. This value is then scaled per Fig. 4 with a modulus taken such that the peak is no greater than  $2\pi$  which avoids overflow issues. Finally this value is once again scaled from  $2\pi$  to 4095 (the C2000 12-bit DAC output maximum) and sent to the C2000 DAC code-generation block.

The hardware for this experiment consists of two Texas Instruments F28379D Control Cards and docks connected to a Teledyne LeCroy HDO8108A Oscilloscope with two Stanford Research Systems FS740 GPS Time Bases that generate a 1 PPS (Pulse Per Second) signal based on UTC from satellite [11] as shown in Fig. 14.

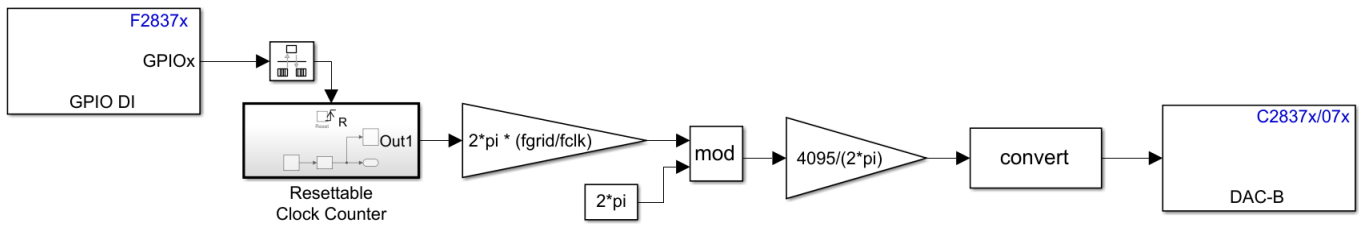


Fig. 7. Simulink Code Generation Model for GPS Time-Discipline

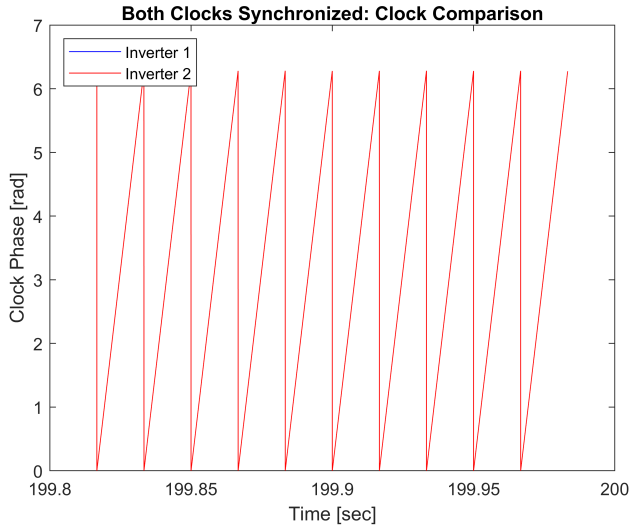


Fig. 8. Case 1 (Both Clocks GPS-Synchronized): Clock Comparison at 200 Seconds

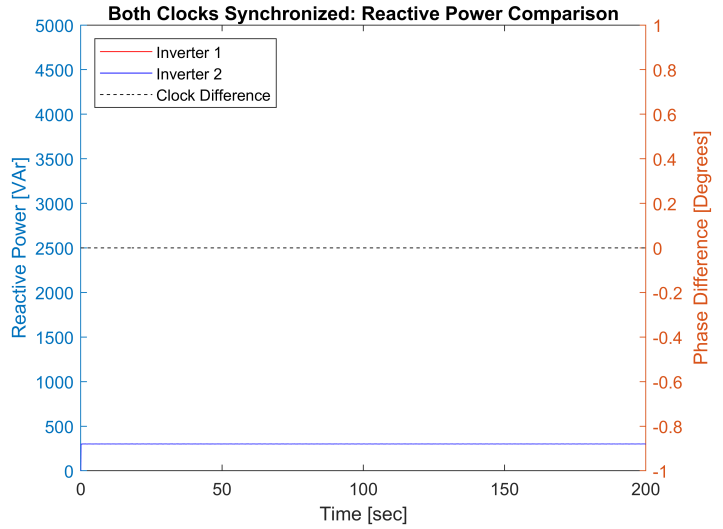


Fig. 10. Case 1 (Both Clocks GPS-Synchronized): Reactive Power Comparison

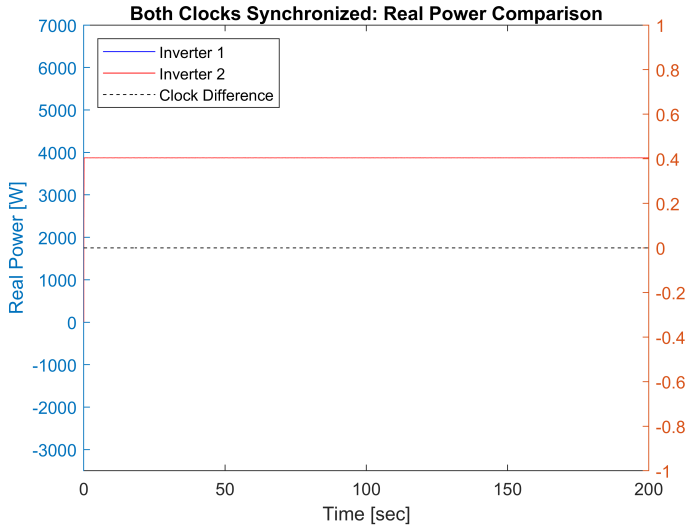


Fig. 9. Case 1 (Both Clocks GPS-Synchronized): Real Power Comparison

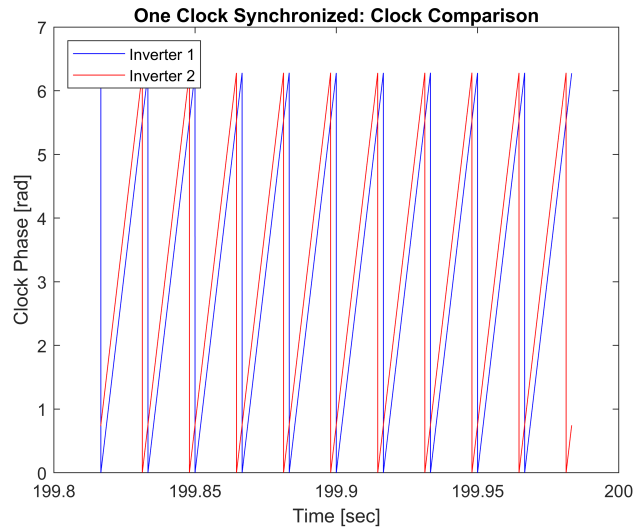


Fig. 11. Case 2 (One Clock GPS-Synchronized): Clock Comparison at 200 Seconds

## VI. EXPERIMENTAL RESULTS

The first test conducted measured the phase difference resulting from the crystal inaccuracies. A GPS pulse was

used to align the microcontroller phase outputs before one microcontroller's GPS connection was removed (Fig. 15).

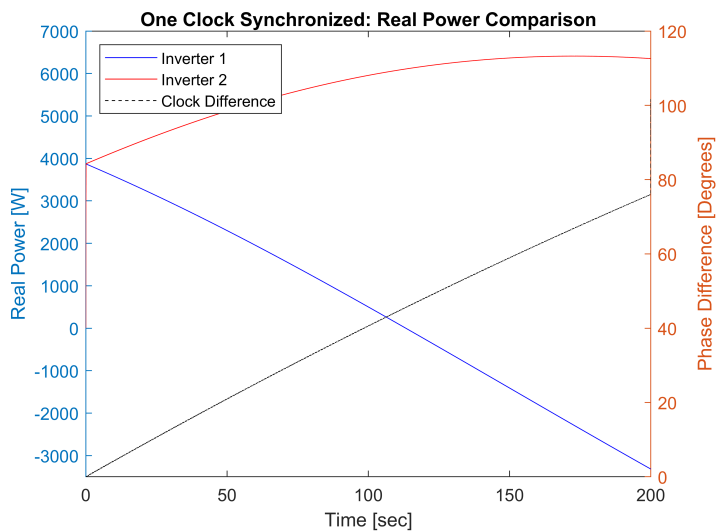


Fig. 12. Case 2 (One Clock GPS-Synchronized): Real Power Comparison



Fig. 14. Physical Hardware Test Setup

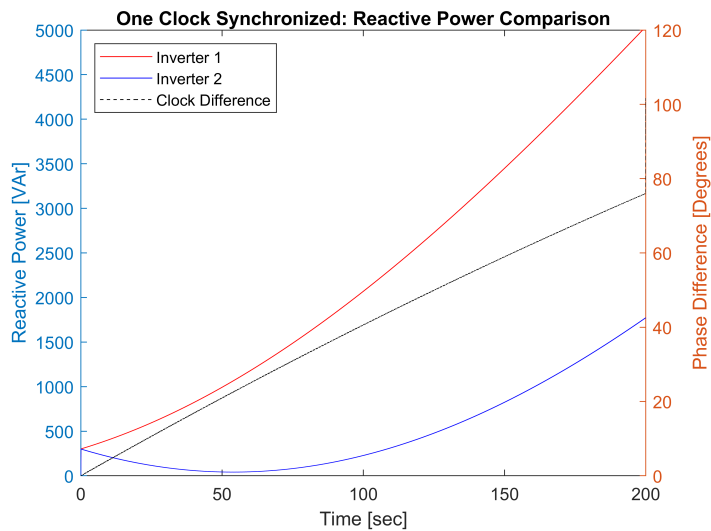


Fig. 13. Case 2 (One Clock GPS-Synchronized): Reactive Power Comparison

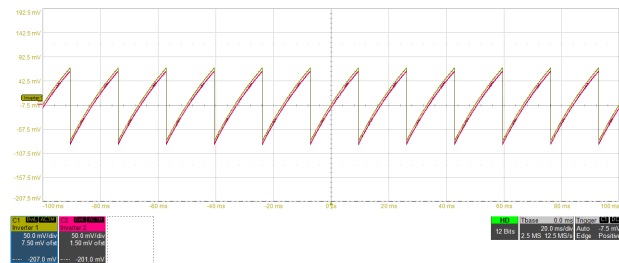


Fig. 15. Initial Phase References.

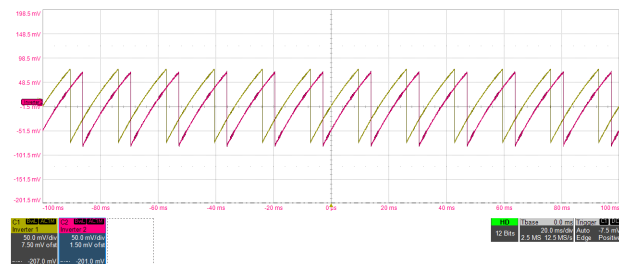


Fig. 16. Phase References after 3.5 Minutes, One is GPS-Calibrated

As calculated in the analysis section, after 3.5 minutes the difference in phase references was approximately 45 degrees out-of-phase (Fig. 16). For the next test, the microcontroller previously disconnected from GPS was reconnected which realigned the reference phases within one second similarly to Fig. 15. At this point, the two GPS-disciplined microcontrollers were run for 72 consecutive hours where they remained precisely aligned for the entire period as shown in Fig. 17.

Comparing the experimentally obtained results with the Simulink simulation phase generator results, it can be seen that the analytically estimated phase shift was observed in the hardware measurement. Specifically, in Fig. 17 and Fig. 8 where both controllers are GPS-synchronized as well as Fig. 16 and Fig. 11 where one clock has crystal drift. By extension, if the tested GPS phase reference controllers were

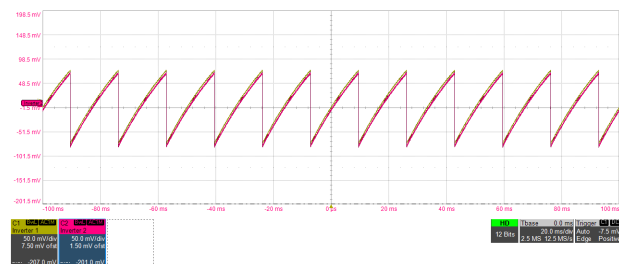


Fig. 17. Phase References after 72 Hours, Both are GPS-Calibrated

implemented in power-level hardware, then the inverters would incur the same phase reference shift observed from simulation.

## VII. CONCLUSIONS AND FUTURE WORK

Droop-based GFMI require a steady internal reference and there are several options to provide this reference but GPS time calibration acts as the most practical method for decentralized, cost-effective applications. The effectiveness of GPS time calibration was proven in this paper through analytical, simulation, and experimental analysis as compared to a standalone microcontroller. Existing methods and frameworks to integrate GPS in GFMI were summarized and the need was demonstrated through this work. By comparing the waveforms over periods of time with and without GPS, it is proven that a form of clock calibration is necessary to maintain GFMI control and prevent power sharing imbalance for GFMI connected to the same load. Optimal applications of this research are future inverter-dominated grids with many decentralized GFMI and renewable energy plants with GFMI connected to shared step-up transformers over long distances. GPS time-synchronization is not optimal for use in systems with facility islands using one reference or systems with several GFMI in proximity that could potentially use alternative synchronization methods (i.e. PTP or MODBUS). Future work in this field involves further scaling these results beyond the presented simple dual inverter system to a distributed inverter-dominated grid.

## VIII. ACKNOWLEDGEMENTS AND DISCLAIMER

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